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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,859	03/08/2004	Jonathon C. Stiff	2059/US/2	2439

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EXAMINER	
HERNANDEZ, WILLIAM	
ART UNIT	PAPER NUMBER
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,859	STIFF ET AL.	
	Examiner	Art Unit	
	William Hernandez	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *4 and 12* is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,5-9,11 and 14* is/are allowed.

6)☒ Claim(s) *10,13 and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's amendment has been received and entered in the case. The amendments and arguments presented therein overcome the indefiniteness rejection, and therefore, it is withdrawn. However, the amendments and arguments do not overcome the prior art rejections, and therefore, these are maintained.

Claim Objections

1. Claims 11 and 14 are objected to because of the following informalities:

In lines 5 of claims 11 and 14, insert the phrase --coupled with the floating current mirror-- after the phrase "a pull-down transistor" as it appears in base claim 10.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 10, 13, 15, 17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Gillingham (USP 5,144,223).

Gillingham's Fig. 5 shows a circuit providing a current reference, comprising:

a floating current mirror including a first transistor (11) and a second transistor (9);

at least one resistor (5 and 6) defining a voltage node;

a pull-down transistor (20) coupled with the floating current mirror (via transistor 7); and

an output transistor (16);

wherein the first transistor is coupled with the at least one resistor and provides an amount of current thereto (transistor 11 is coupled to resistor 5 via transistor 8);

wherein the second transistor is coupled with the output transistor for providing a bias signal to the output transistor (transistor 9 is coupled to the gate of output transistor 16 via inverter 15); and

wherein the amount of current provided by the first transistor into the at least one resistor is mirrored to the second transistor (resistors 5 and 6 are coupled in series with transistor 11 with no diverting paths in-between); and

wherein the first and second transistors are p-channel MOSFETS (clearly shown) as called for in claim 10.

Regarding claim 13, Gillingham's Fig. 5 shows the circuit of claim 10, wherein the amount of current mirrored to the second transistor provides a bias signal to the output

transistor (current flows through second transistor 9 towards the output transistor 16's gate, providing a bias signal).

Regarding claim 15, Gillingham's Fig. 5 clearly shows the recited limitation (also see col. 4: 43-44).

Regarding claim 17, Gillingham's Fig. 5 shows the circuit of claim 10, further comprising:

a protection transistor (8) coupled between the pull-down transistor and the floating current mirror.

Regarding claim 19, Gillingham's Fig. 5 shows the circuit of claim 10, wherein a load (19, 20 and 21) is coupled to the output transistor, the load receiving the current reference.

4. Claims 10, 15 and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobatake (USP 6,204,724 B1).

Kobatake's Fig. 8 shows a circuit providing a current reference, comprising:

a floating current mirror including a first transistor (P2) and a second transistor (P1);

at least one resistor (R1) defining a voltage node;

a pull-down transistor (N25); and

an output transistor (P3);

wherein the first transistor is coupled with the at least one resistor and provides an amount of current thereto (transistor P2 is coupled to resistor R1 via transistor N2);

wherein the second transistor is coupled with the output transistor for providing a bias signal to the output transistor (transistor P1's gate is coupled to the gate of output transistor P3); and

wherein the amount of current provided by the first transistor into the at least one resistor is mirrored to the second transistor (I_2 and I_1 are mirrored currents); and

wherein the first and second transistors are p-channel MOSFETS (clearly shown) as called for in claim 10.

Regarding claim 15, Kobatake's Fig. 8 clearly shows the recited limitations.

Regarding claim 17, Kobatake's Fig. 8 shows the circuit of claim 10, further comprising:

a protection transistor (P27) coupled between the pull-down transistor and the floating current mirror.

Regarding claim 18, Kobatake's Fig. 8 clearly shows the recited limitation.

Regarding claim 19, Kobatake's output transistor is clearly capable of being coupled to a load, the load then receiving the current reference.

5. Claims 10, 13, 15, 16 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Morishita et al. (USPAP 2004/0027194 A1).

Morishita et al.'s Fig. 11 shows a circuit providing a current reference, comprising:

a floating current mirror including a first transistor (21) and a second transistor (22);

at least one resistor (R1) defining a voltage node;

a pull-down transistor (24) coupled with the floating current mirror; and

an output transistor (NTT);

wherein the first transistor is coupled with the at least one resistor and provides an amount of current thereto (transistor 21 is coupled to resistor R1 via transistor 23);

wherein the second transistor is coupled with the output transistor for providing a bias signal to the output transistor (transistor 22 is coupled to the gate of output transistor NTT); and

wherein the amount of current provided by the first transistor into the at least one resistor is mirrored to the second transistor (i_0 and i_1 are mirrored currents); and

wherein the first and second transistors are p-channel MOSFETS (clearly shown) as called for in claim 10.

Regarding claim 13, Morishita et al.'s Fig. 11 shows the circuit of claim 10, wherein the amount of current mirrored to the second transistor provides a bias signal to the output transistor (current flows through second transistor 22 towards the output transistor NTT's gate, providing a bias signal).

Regarding claims 15 and 16, Morishita et al.'s Fig. 11 clearly shows the recited limitations.

Regarding claim 19, Morishita et al.'s output transistor is clearly capable of being coupled to a load, the load then receiving the current reference.

Response to Arguments

6. Applicant's arguments filed 9/18/06 have been fully considered but they are not persuasive.

7. Regarding amended claim 10, applicant alleges that claim 12 was allowed by the Examiner, and as a result, claim 10 would be allowable for including the limitations of claim 12. In fact, claim 12 was rejected under Gillingham, Kobatake and Morishita et al. in the previous office action (6/16/06); thus, the rejection of claim 10 is maintained.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Hernandez whose telephone number is (571) 272-8979. The examiner can normally be reached on Mon.-Fri. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WH

WH 1/8/07

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